# CSE 531: Distributed and Multiprocessor Operating Systems

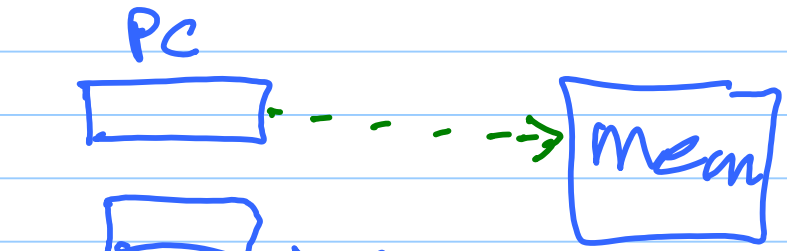
Fall 2020

Class: 03 Date: 8/31

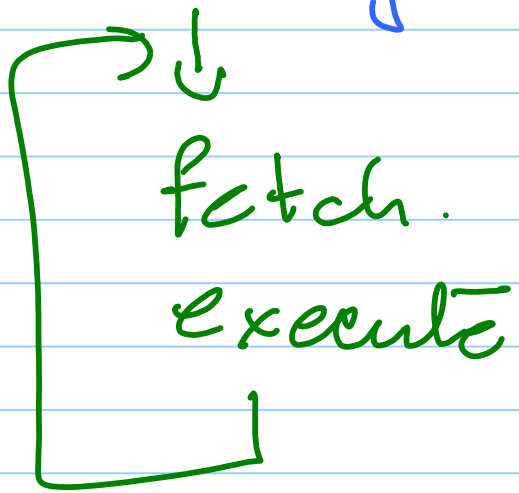
Note Title

Single CPU

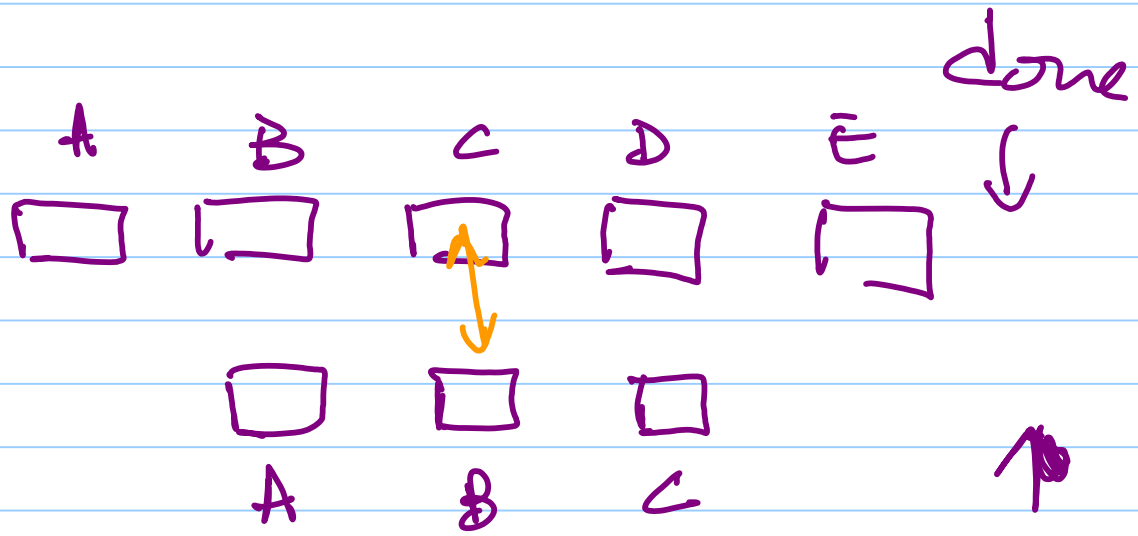
- single cycle CPU




all software assume CPUs are single cycle

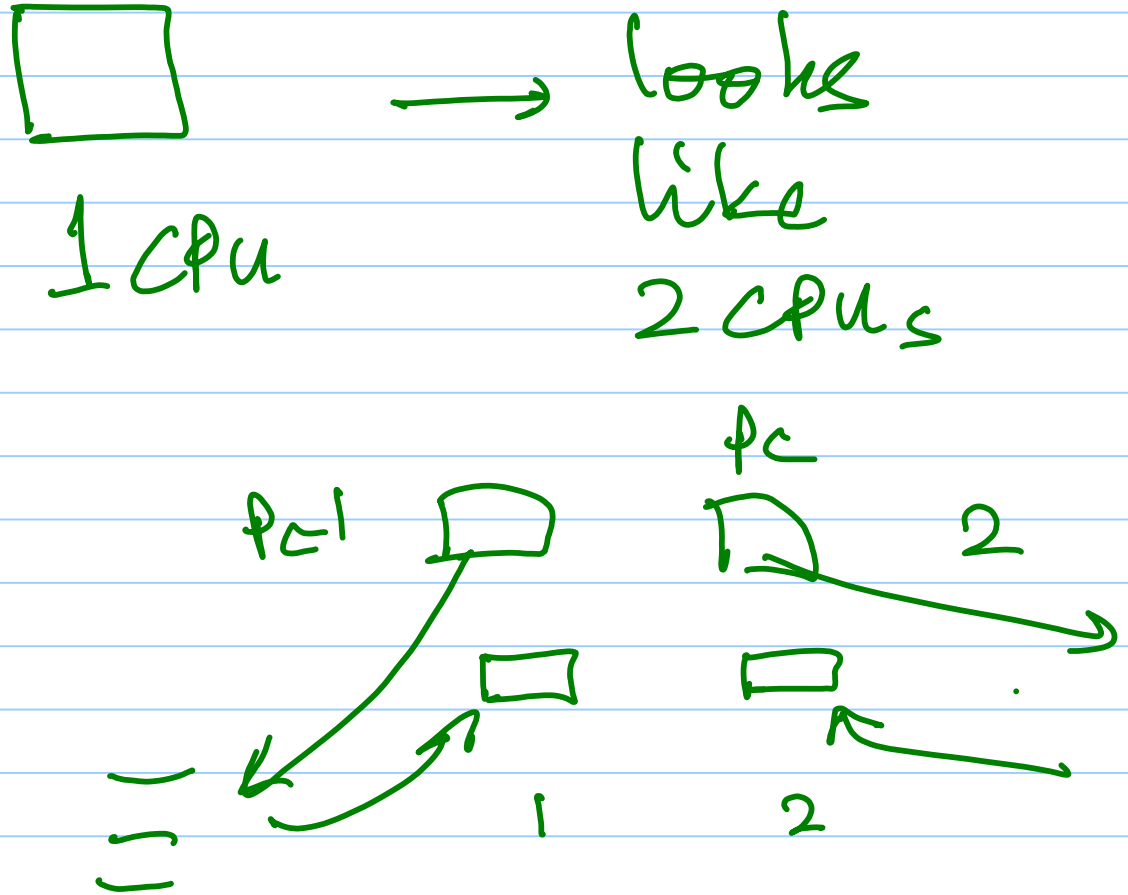


- Single cycle
- cache → intermediate...
- pipelining

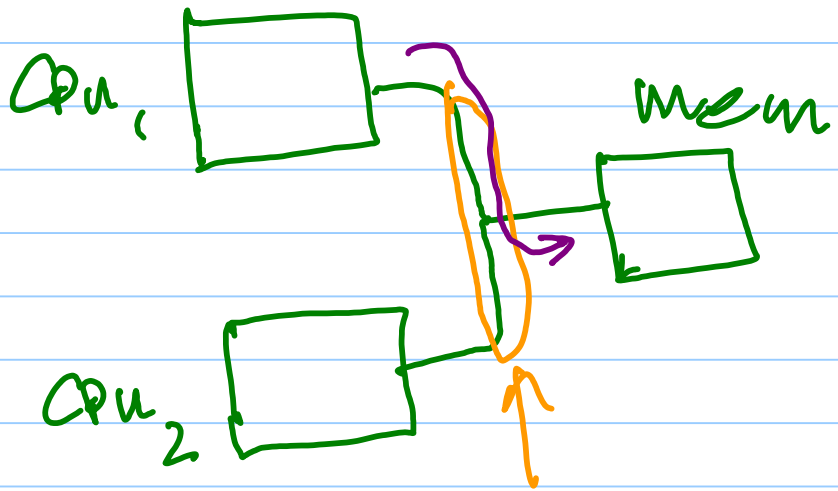



- hyperthreading

hyper



# UMA architecture



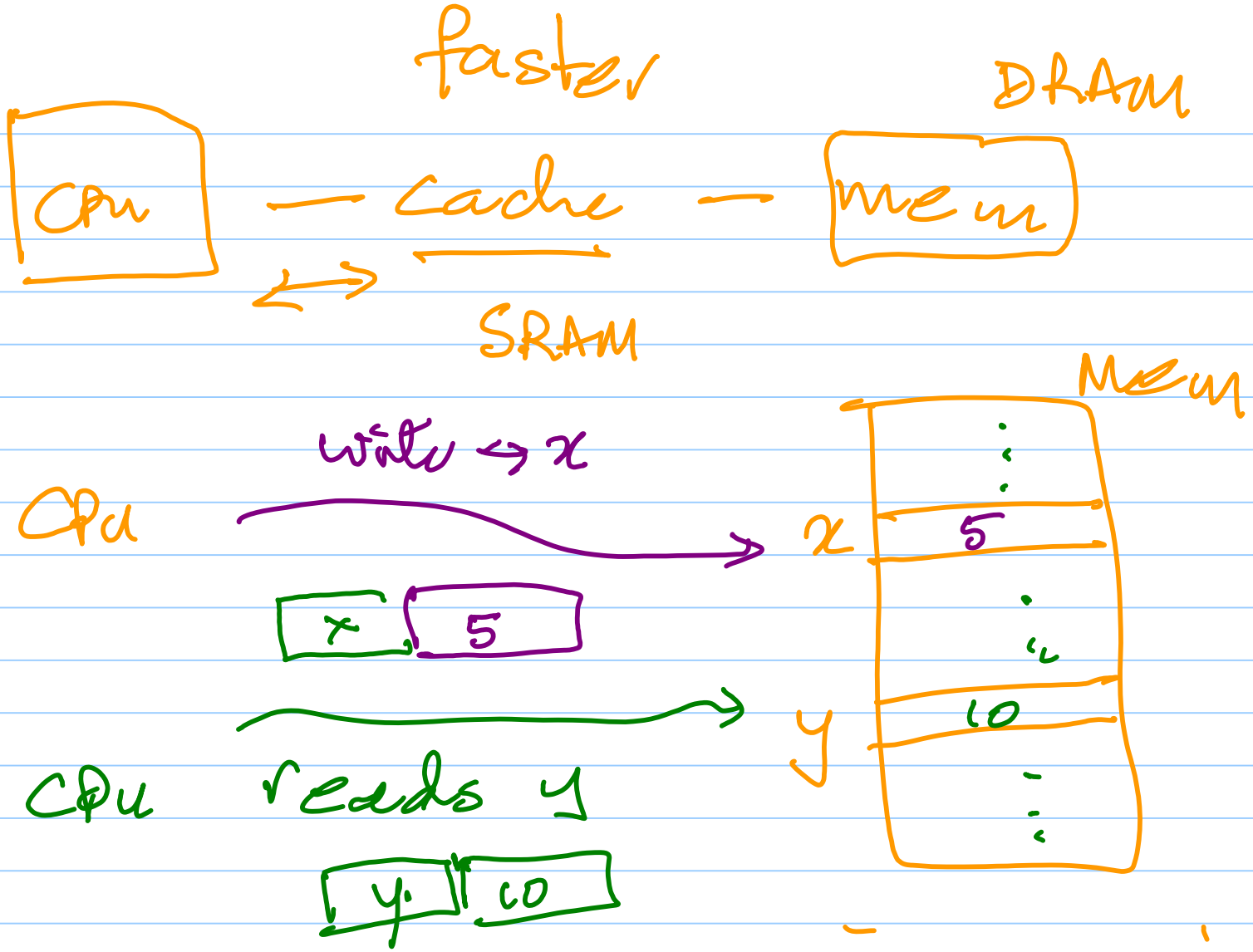

contention

cycle

1 fetch → mem R

≥1 execute → ?

2 accesses/cycle


faster
DRAM
CPU
cache
mem
SRAM
Mem
write x
CPU
x
5
CPU reads y
y
10

# Cache lookup

CPU ⟶ addr to cache

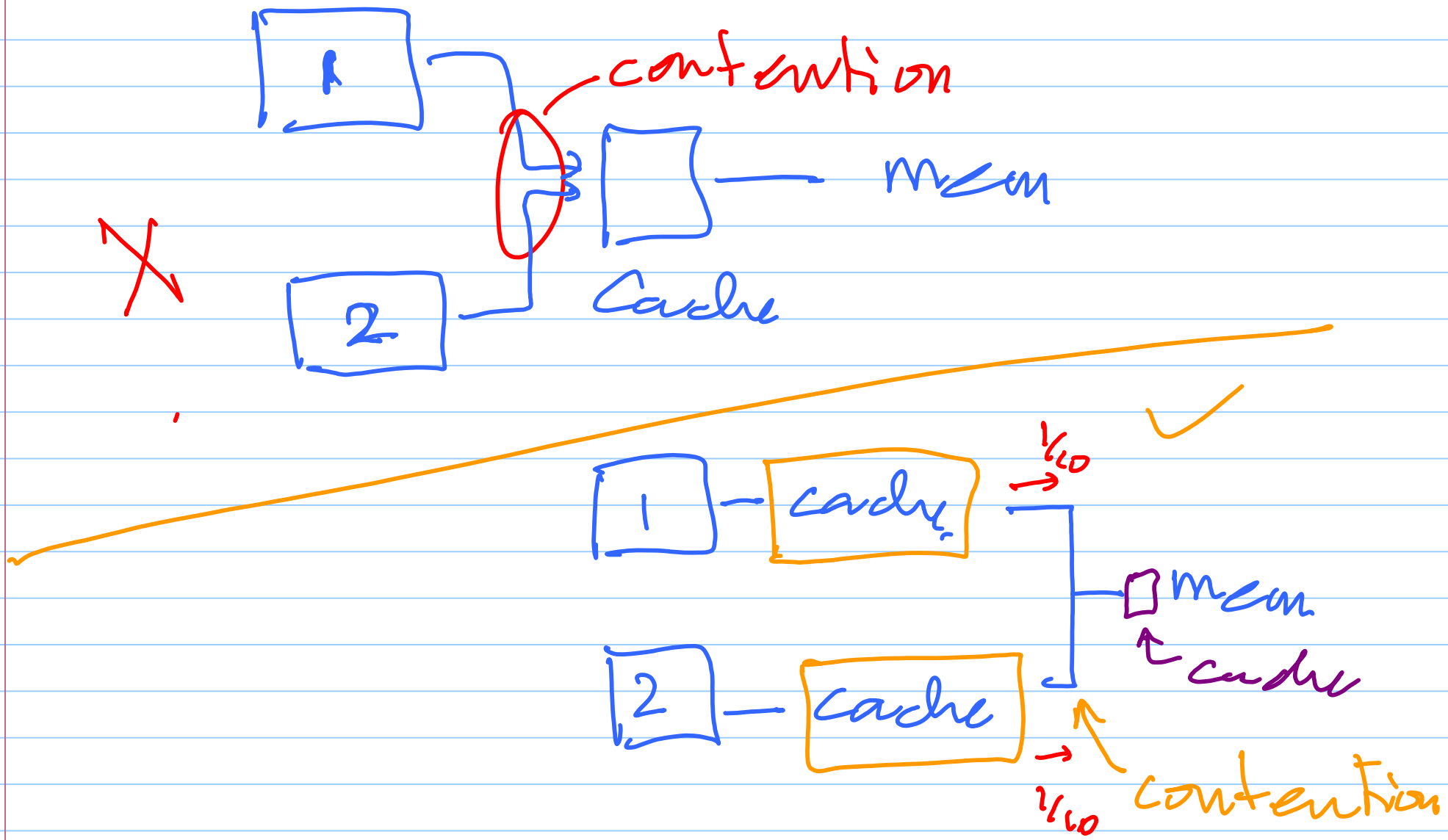
↓

Search tags for addr

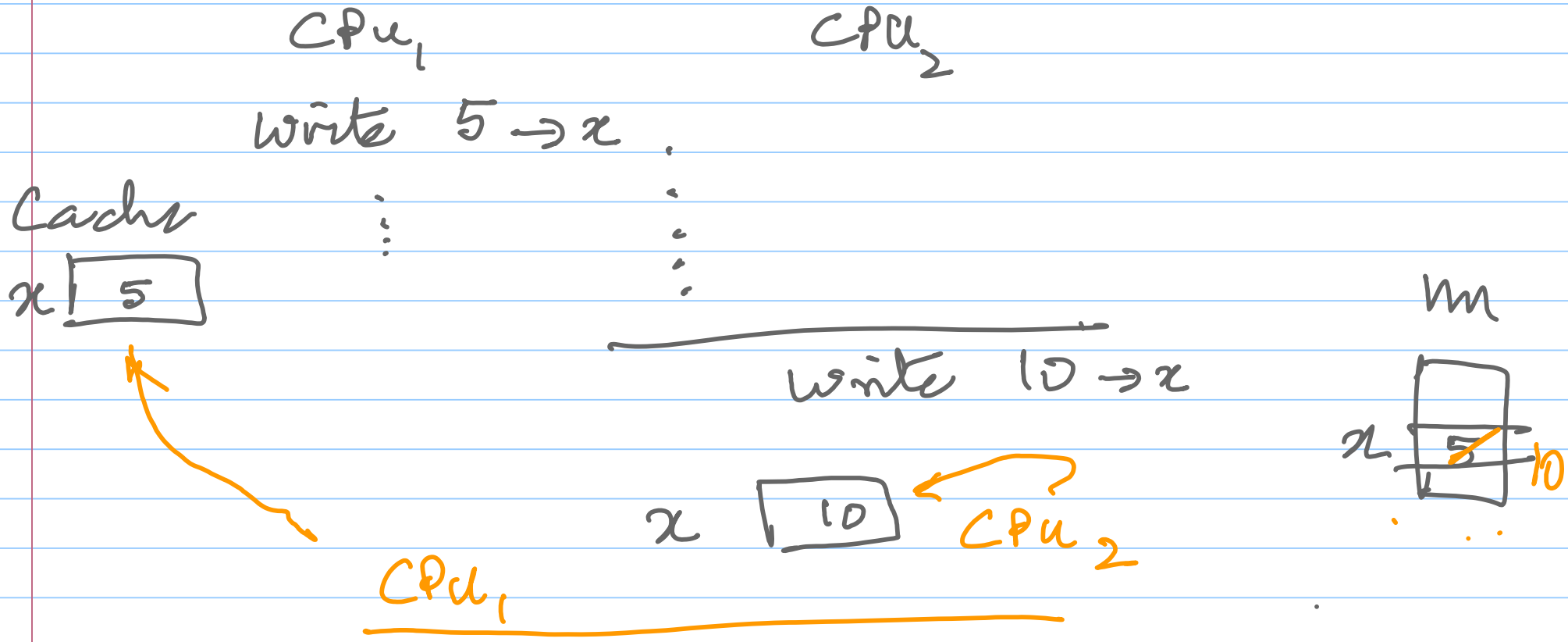
↳ exists → HIT

→ no " — MISS

# Multi CPU + cache



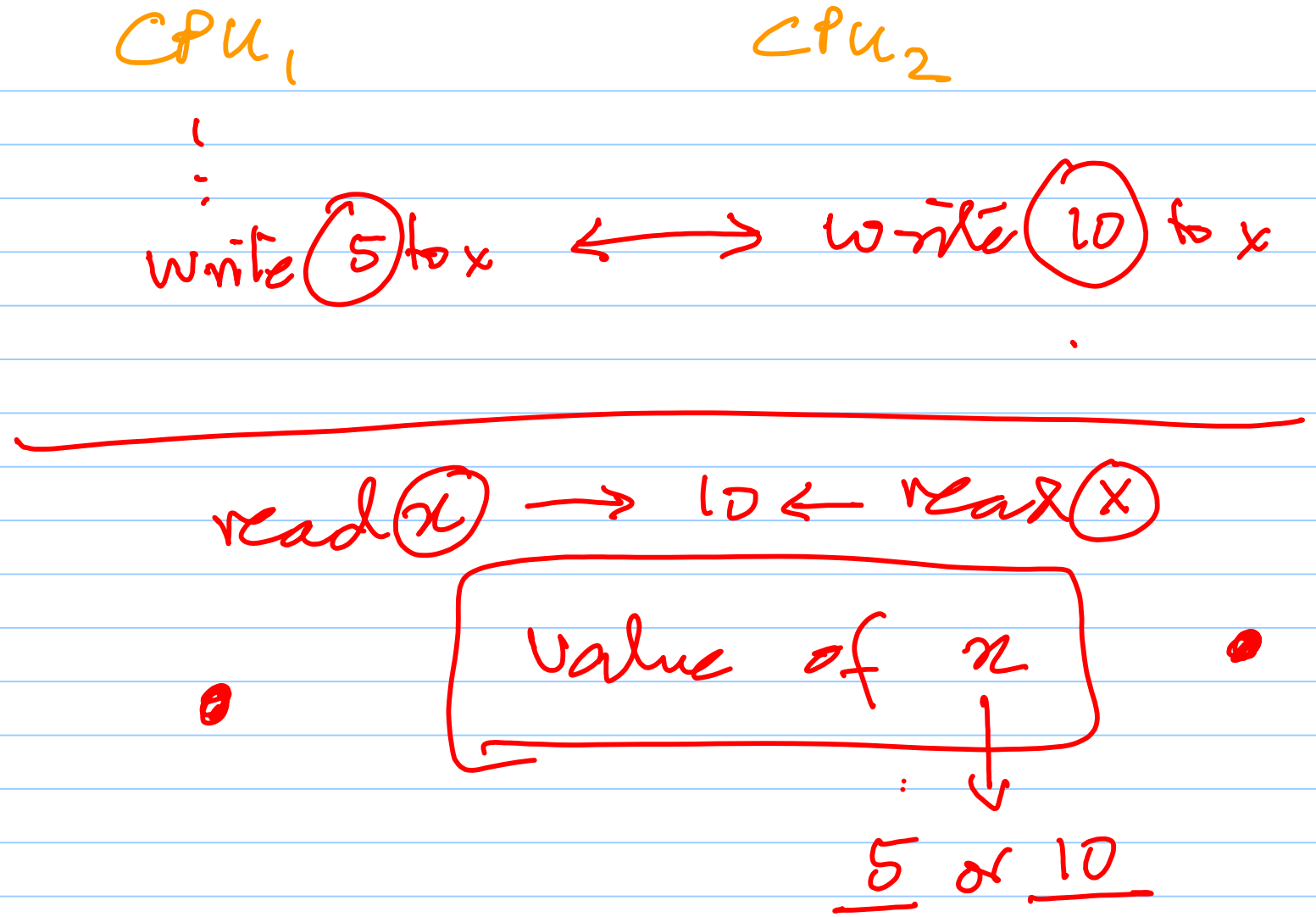
# problem → cache coherency



non coherent caches

→ use programming to solve the problem

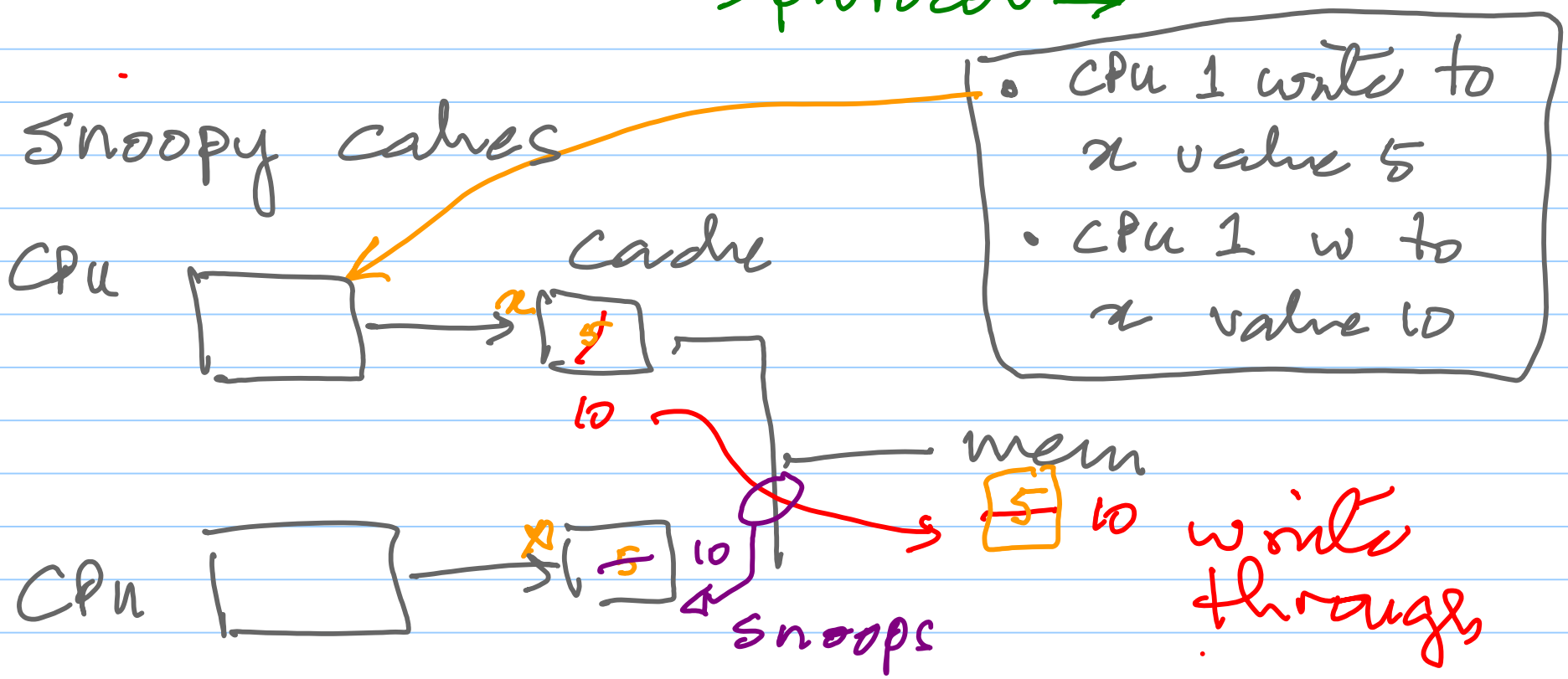
every read returns the most recent write


CPU1
CPU2
write 5 to x
write 10 to x
read x
10
read x
value of x
5 or 10

# Coherent caches

(cache coherency)

→ protocol →



Coherent caches

→ snoopy

↓

performance degrades (but better than no cache)

→ does not scale

# NUMA




NORMA X

# NUMA

- Scalable
- high performance
- special appl
  - ↳ 1 appl / machine / time

# CC-NUMA

Cache coherent NUMA

↳ NUMA that look like UMA