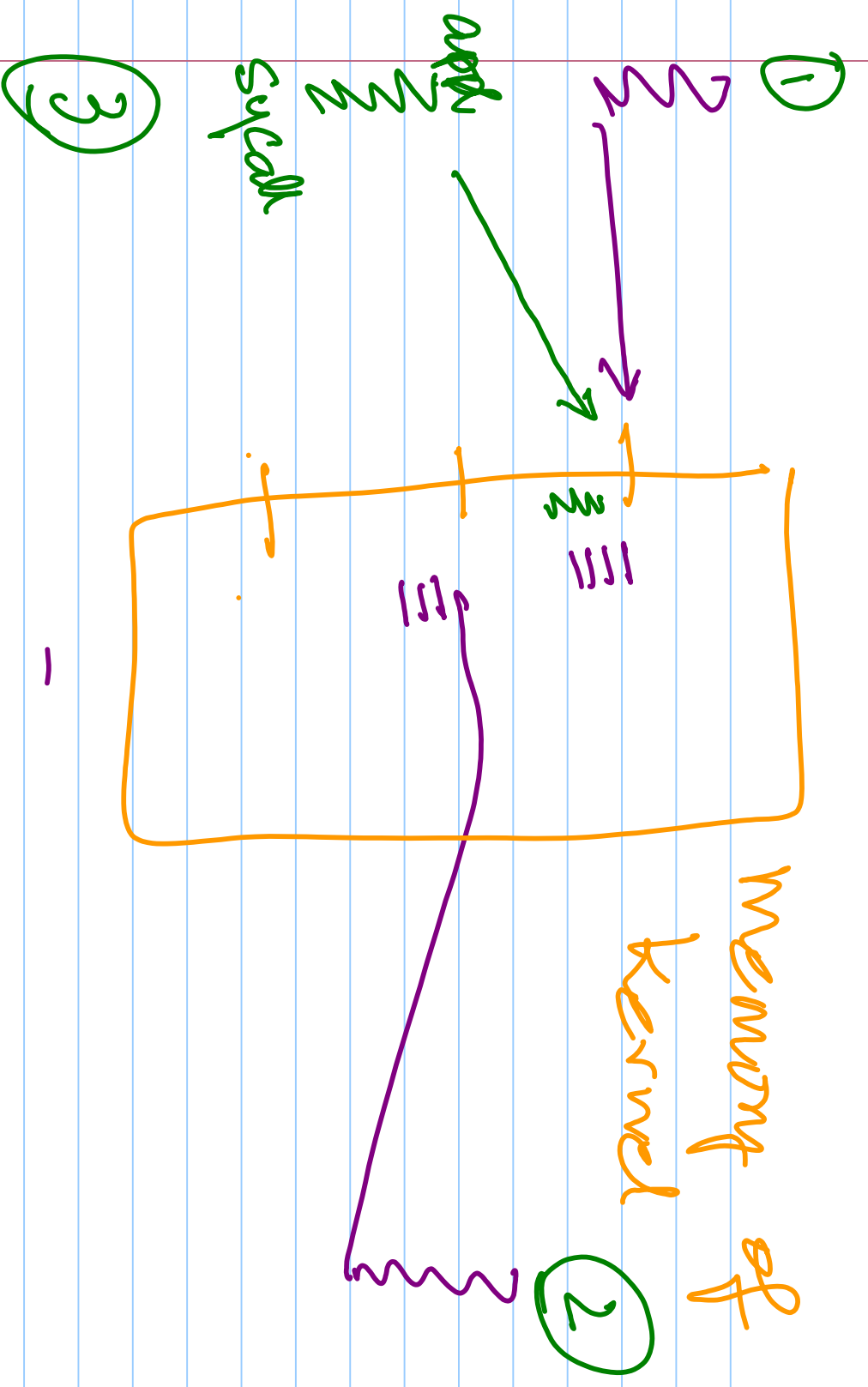
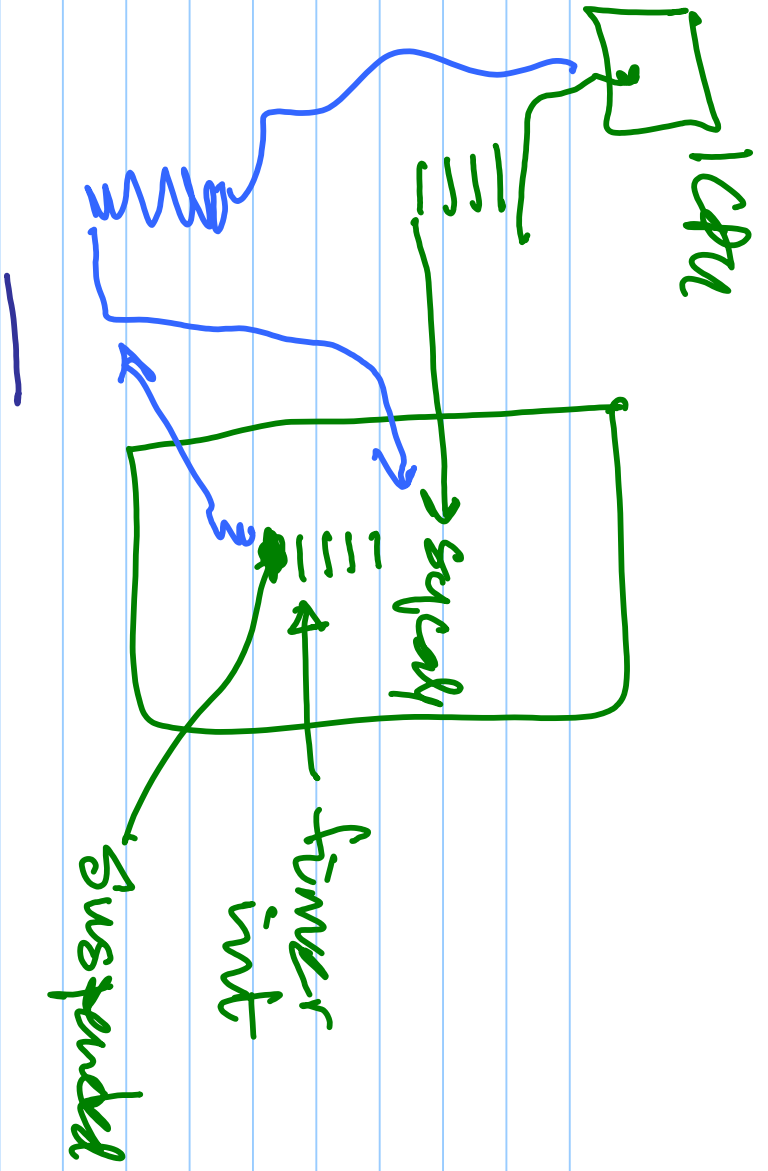


—



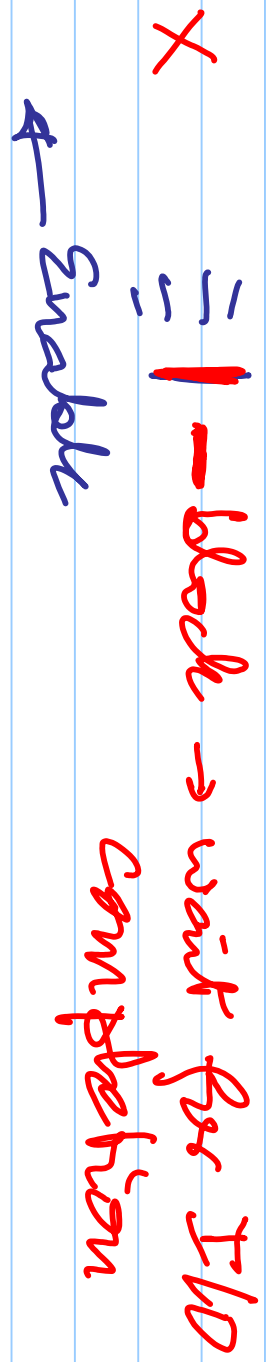


1

Single CPU kernel

→ Disable Int while kernel executes

→ disable



Non Preemptive Kernel

→ Do not context switch

→ kernel

→ flag ← do not context switch

∴ → can be made to work
∴

BigLock

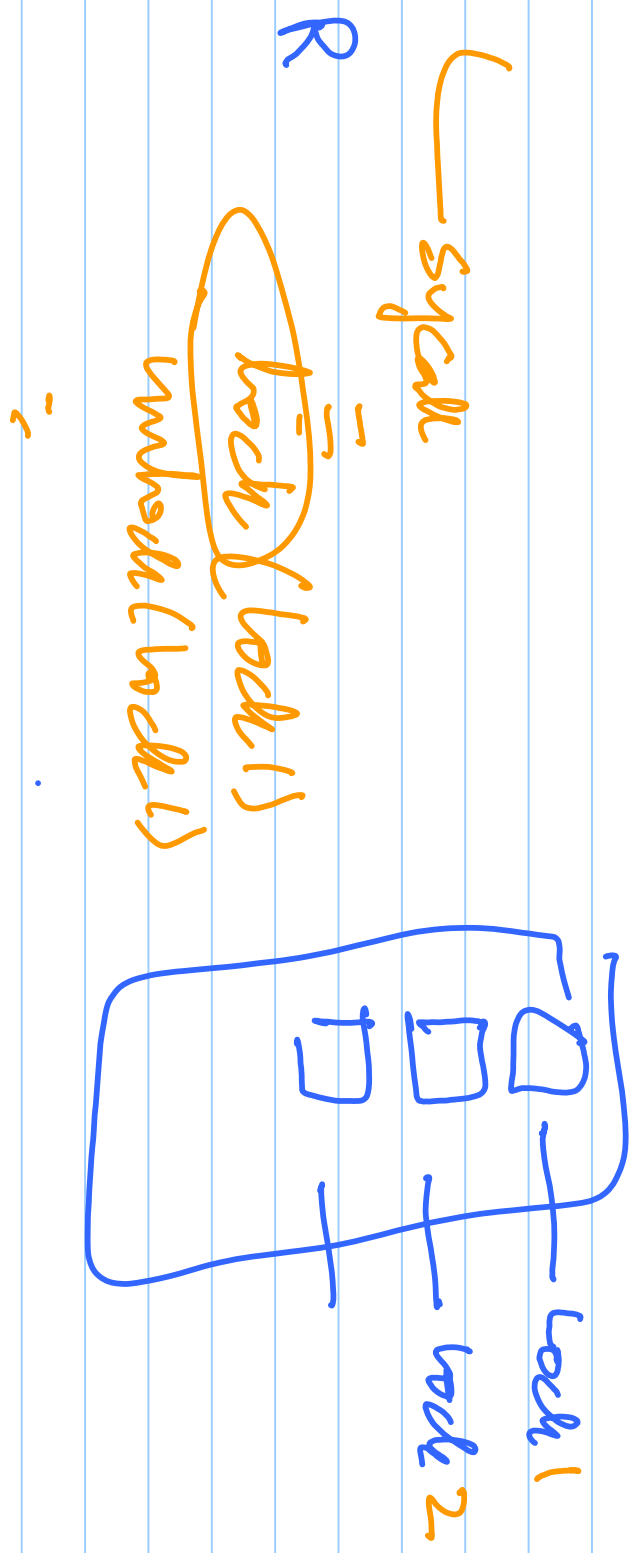
→ lock (kernel lock)

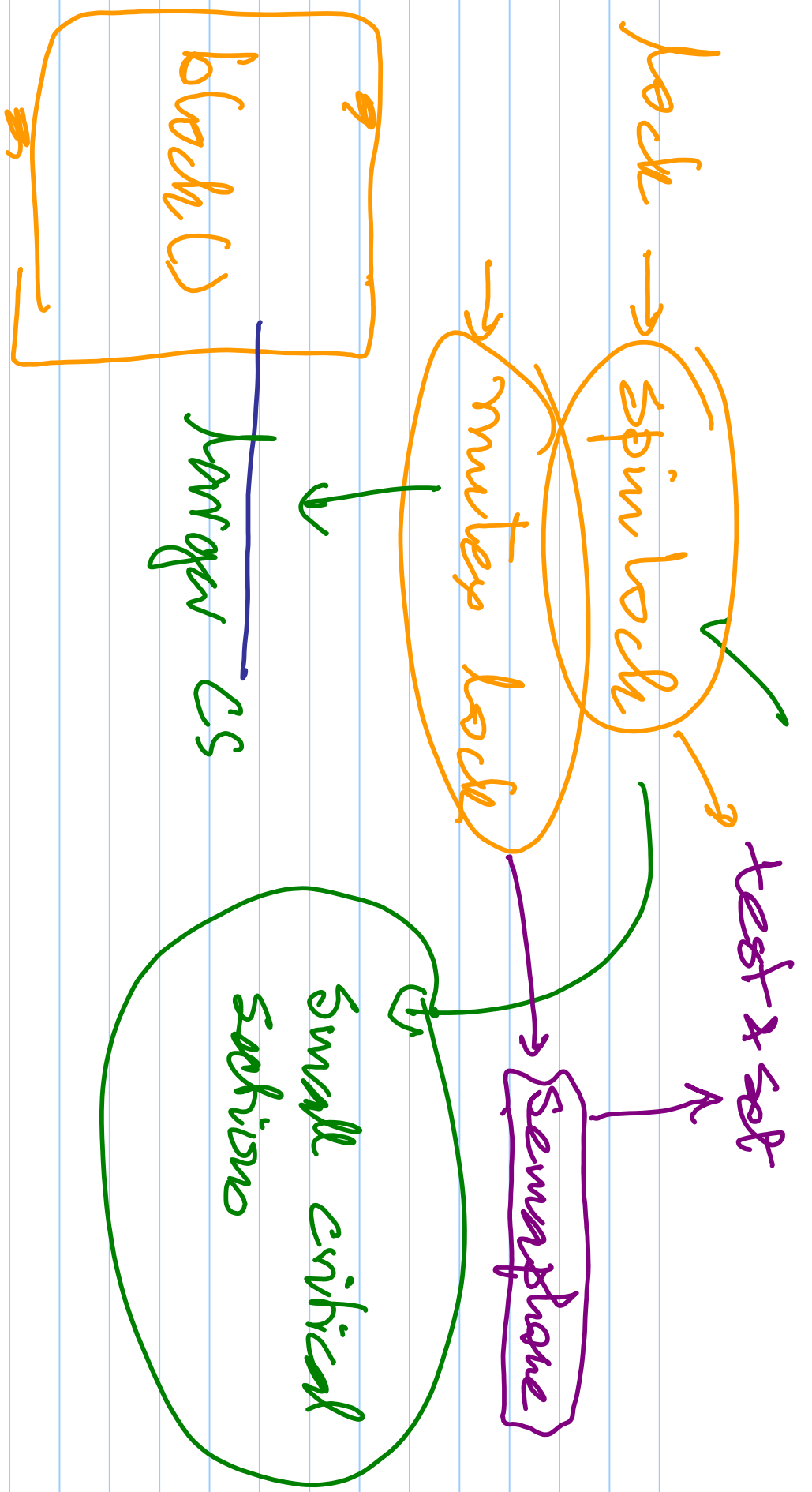
┌
┌
┌

○ unblock

① preemptible kernel

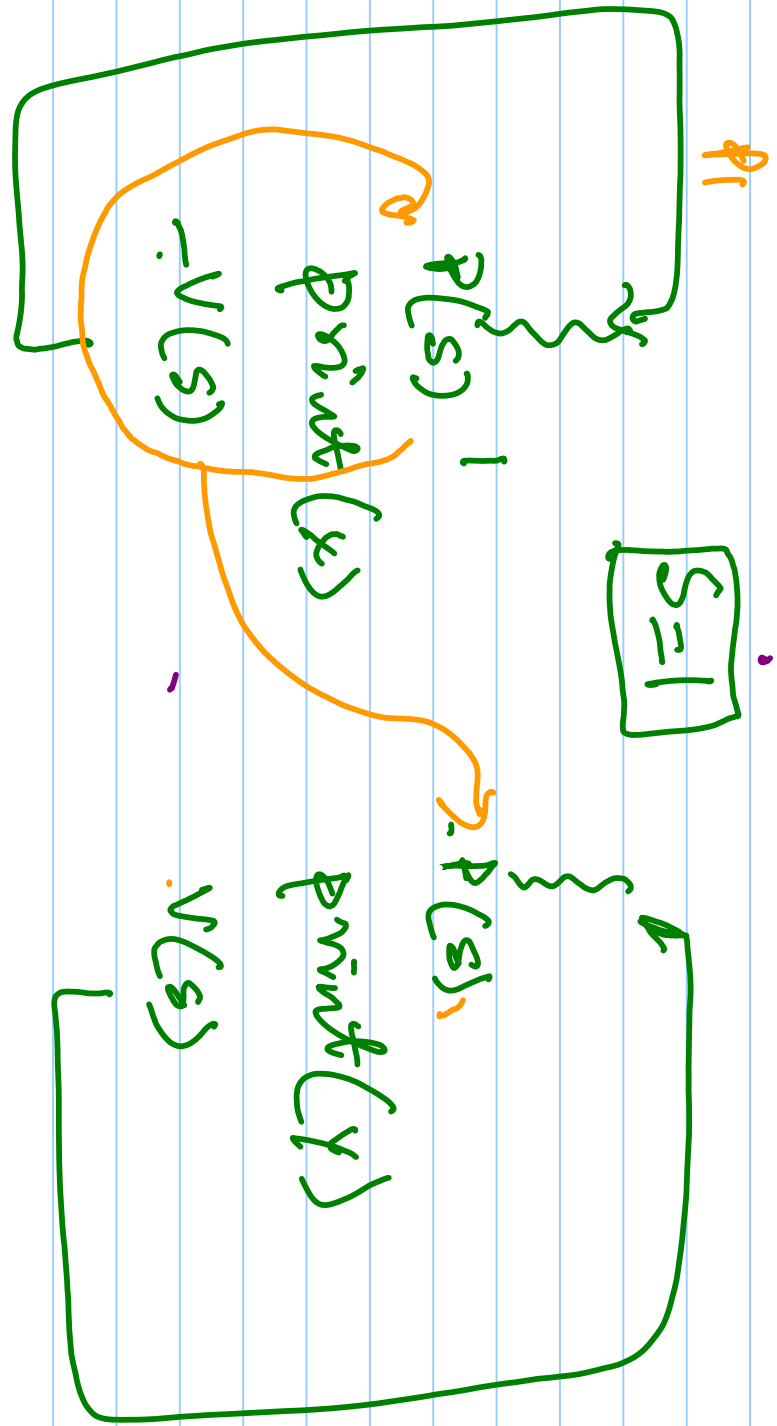
② fine grain locks



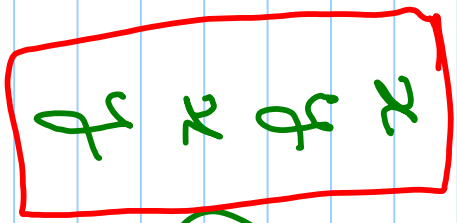


Semaphores as mutex locks

→ done?



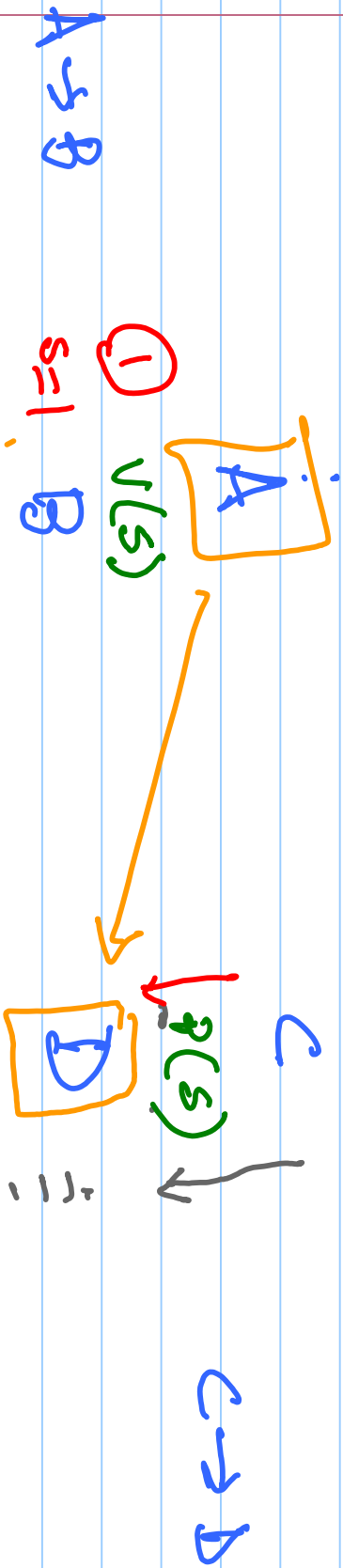
x x y x x y



(?)

Synchronization

P_1 $S=0$ P_2



D can happen only after A is completed

$S_1 = 0$ $S_2 = 1$

y
 $f(S_2)$
Print(x)
 $v(S_1)$

$v(S_1)$
Print(y)
 $v(S_2)$

→ x will print 1st, followed by y, x, y, x

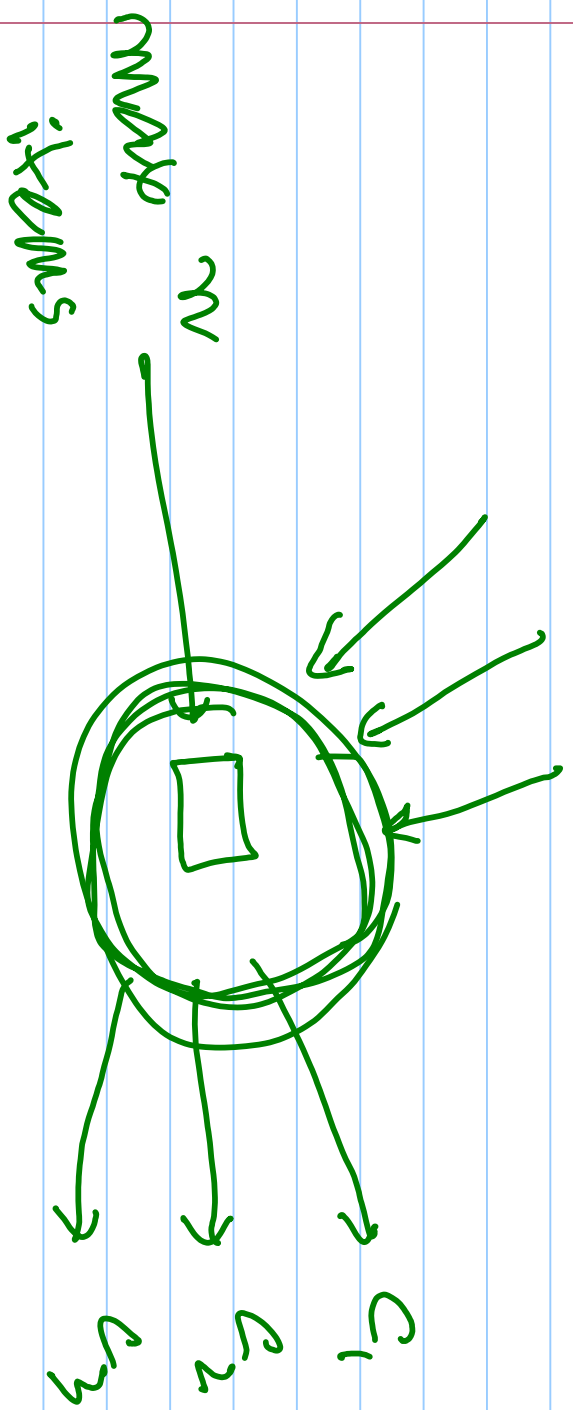
$S_1 = 0$ $S_2 = \frac{1}{2}$ 0

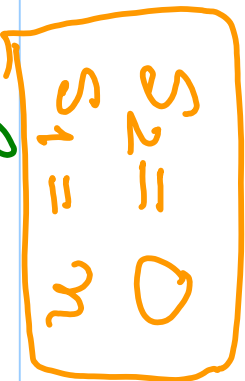
\rightarrow print(x)
v(s₁) ,
P(s₂)

P(s₁) \leftarrow
print(y)
v(s₂)

Producer - Consumer (aka

P_1, P_2, P_3 bounded buffer)





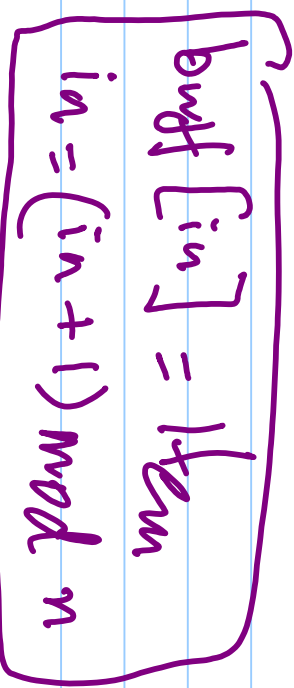
Producer

$P(s_1)$

↓ ↓ put in buffer

$V(s_2)$

buff[in]
in == 0 out == 0



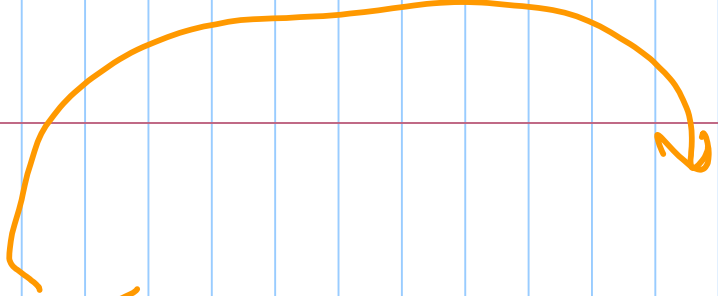
Consumer

$P(s_2)$

take from buffer ↓

$V(s_1)$

item = buff[out]
out = (out + 1) mod n



Prod

Cons

1 prod, 1 cons \rightarrow works

1 multiple prod / cons race condition

$P(bsum)$

$\downarrow \downarrow$

buff[n] = item1 item2

$V(bsum)$

CS

P - Sample

$$\begin{matrix} S_1 = n \\ S_2 = 0 \end{matrix}$$

$$P(S_i)$$

$$\approx \text{buff}$$

$$V(S_2)$$

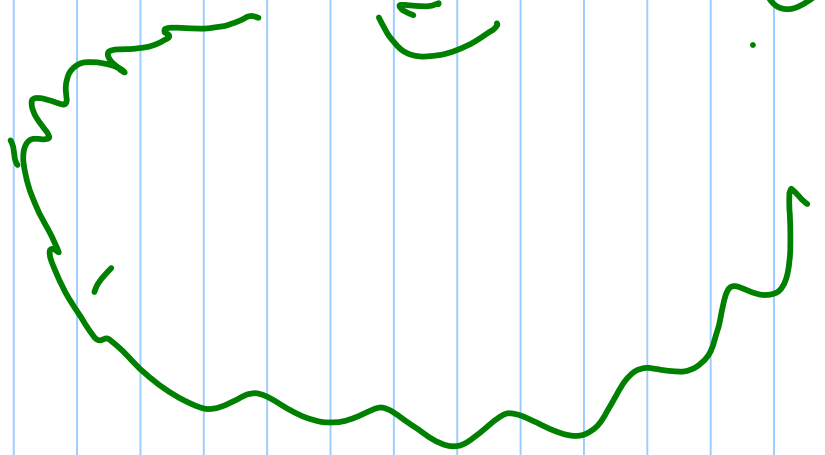
buff₀, buff₁, ...

C - Sample

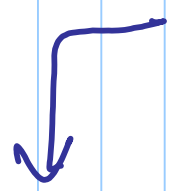
$$P(S_2)$$

$$\approx$$

$$V(S_1)$$

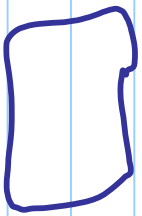


- Checking values of
Semaphores?

$P(s)$  NSO!

Prod

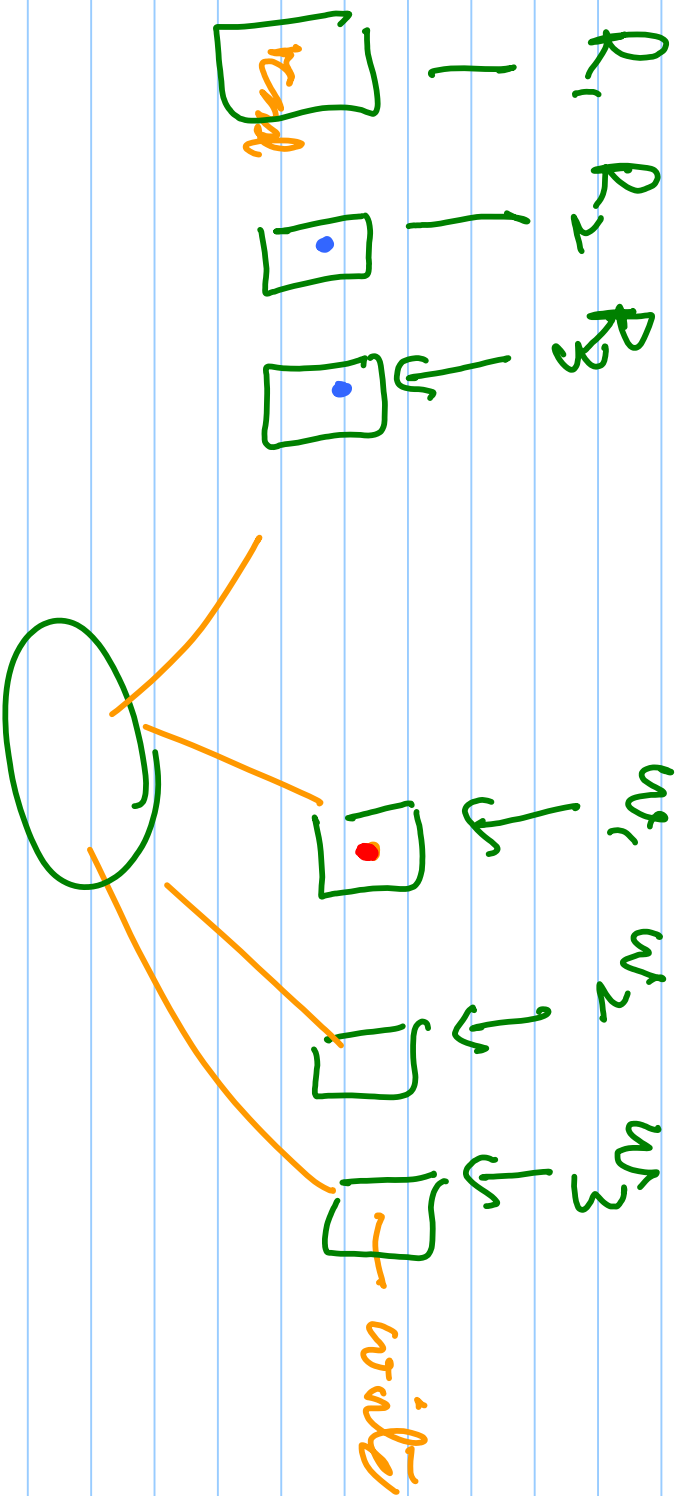
$P(S_i)$



count++

$V(S_2)$

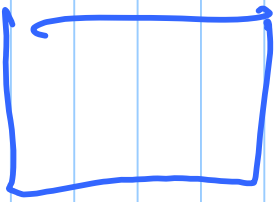
Readers + Writers



Multiple readers OR single writer

Reader

R - entry code



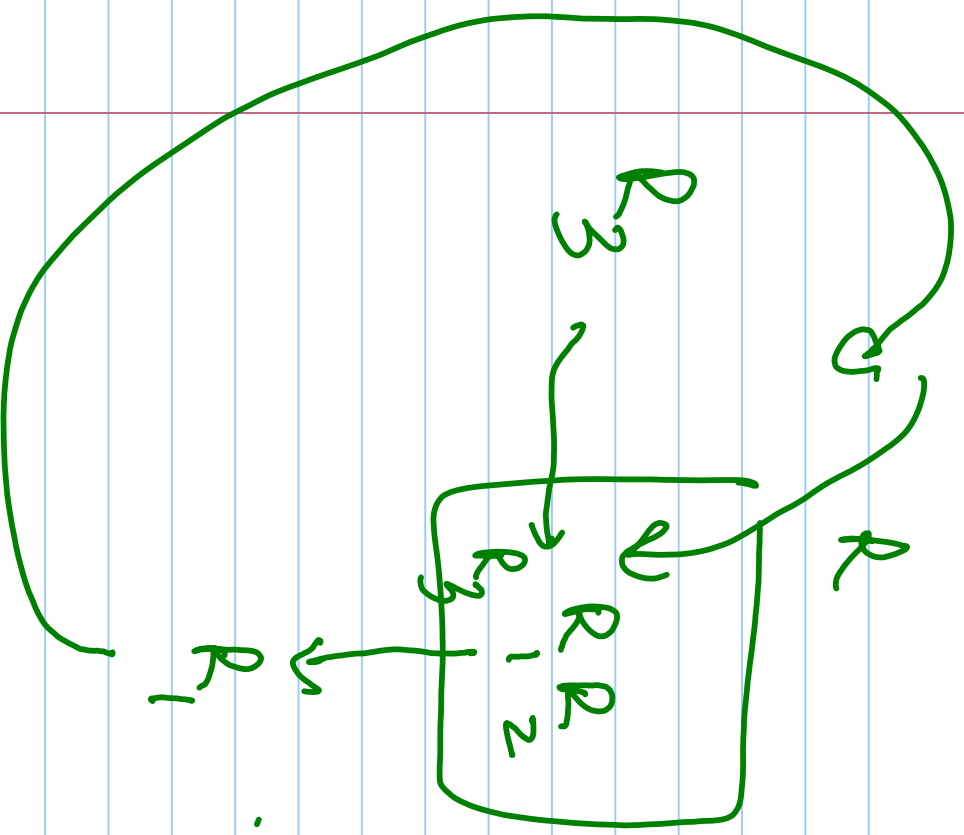
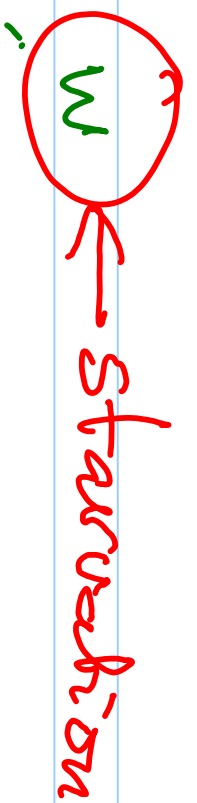
R - exit code - V(s)

$s = 1$

w

$P(s)$

$V(s)$



① if w is waiting
new readers are
not allowed to
enter

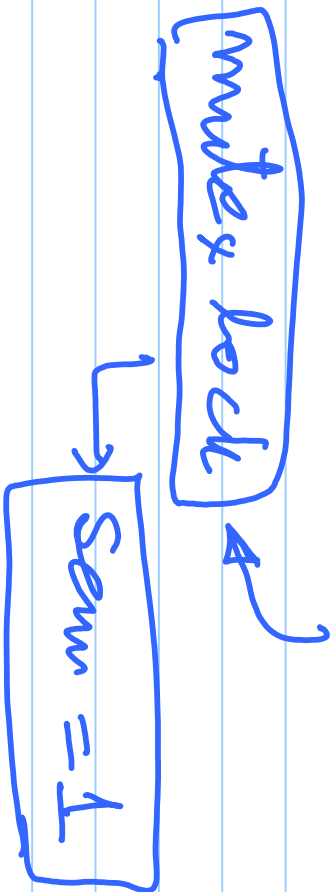
② last R out must
give w preference

③ w exit makes
all waiting R
enter at same time

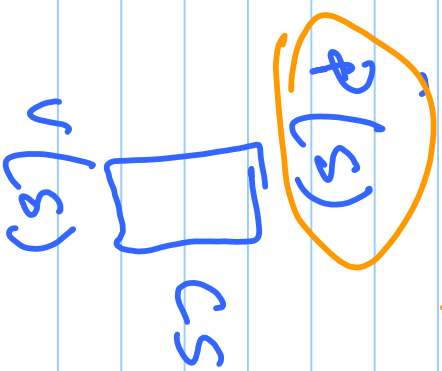
Mutex

mutex \rightarrow phrasalo.

data struct



mutex



pthread

